Thermal Analysis Simulation Report on “Test Board”

Date:	….
Client:	….
Contact:	…
Order Number:	…
Quote:	…
Report Version:	Sample results
Software Version:	TRM x.x

Content

1 Input Data and Specification

1.1 Scope of investigation

… Reproduction of your request and individual input data …

Mail from …:

1.2 Power conditions

Power by fixed values

- U1 = 0.5 Watt
- U2 = 0.5 Watt
- U3 = 0.5 Watt

1.3 Electric conditions and schematics

- Net 1 @ 8 A: from pin J2_1 to pin J1_2. DC.

1.4 Gerber files

105-00069.GBL
105-00069.GTL
105-00069.GTO
105-00069.DRL

1.5 Layer stack

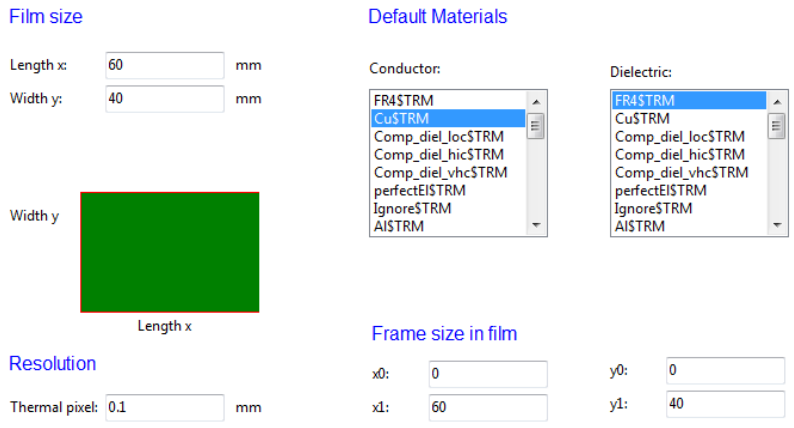
1.6 Environmental and cooling conditions

- 20 degC ambient air temperature
- free convection, laboratory setup

2 Board Model

2.1 Board size and default materials

Finest trace lines are at 0.2 mm: set thermal pixel size to 0.1 mm.



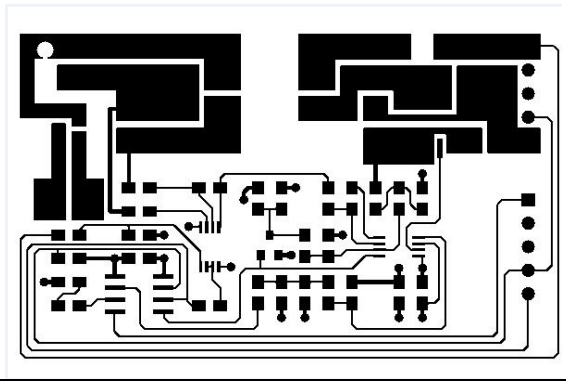
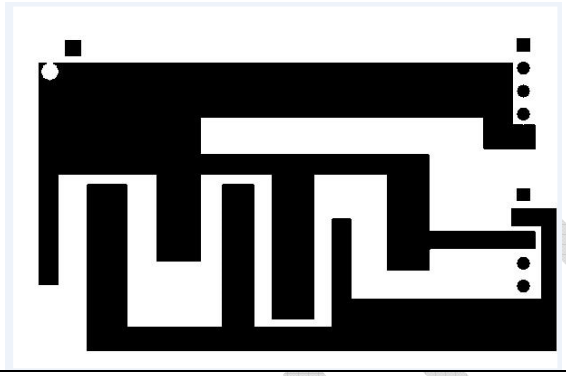
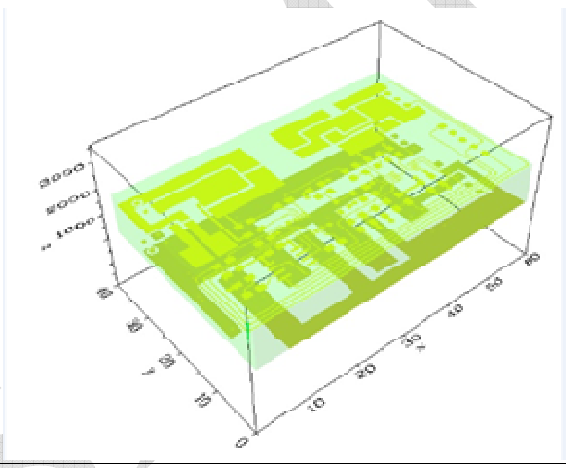
Optional comments
….

2.2 Layer stack

A board model is build-up by ‚Levels‘, which could contain a copper pattern or not.
2 component levels are internally added: 00 and 04.
Those numbers also will appea in result plots.

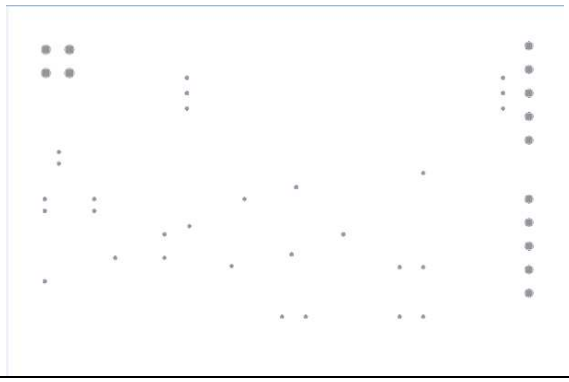
Name	Type	File	View	FR4 white?	Thick (mu)	Conductor	Dielectric
Top	ger	105-00069.GTL	View	☑	35	Cu$TRM	FR4$TRM
Core	pre		View	☑	1530	Cu$TRM	FR4$TRM
Bottom	ger	105-00069.GBL	View	☑	35	Cu$TRM	FR4$TRM

2.3 Layout drawings

	Top layer 105-00069.GTL
	Bottom layer 105-00069.GBL
	3D impression

2.4 Drill pattern

- All holes are copper plated w/20 microns
- All drill are through holes

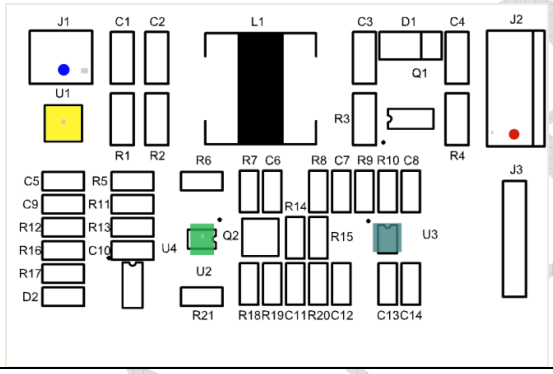


Drills
105-00069.DRL

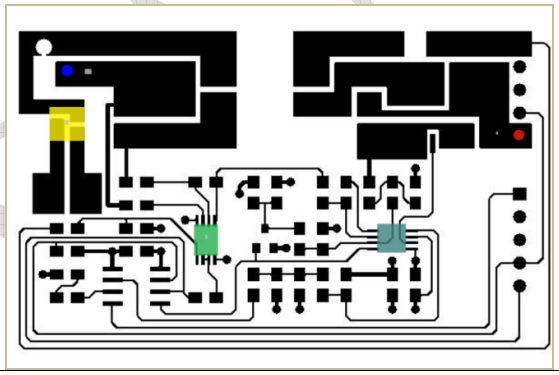
Type	Drillfile	View	Tech	z-Begin	z-End	Plated	Ring (mu)	Ring material	Filled?	Fill material
cnc	105-00069.DRL	View	TH	0	100	☑	25	Cu$TRM	☐	

2.5 Components and pins

- Components are quads with a homogeneously distributed power loss and
- have a mixed value of thermal conductivity 10 W/mK (empirical).
- …



Circles: pins
Rectangles: components



Index	Name	Posx (mm)	Posy (mm)	Dimx (mm)	Dimy (mm)	Height (mm)	z-Begin	z-End	Material	Form	K/W-board	K/W-air	Watt	Celsius	Ampere
0	MINUS	6.604	32.779	1.27	-1	2	-1	-1	Cu$TRM	c	-1	-1			-8
1	PLUS	56.157	25.695	1.167	-1	2	-1	-1	Cu$TRM	c	-1	-1			8
2	MINUSpin	6.604	32.779	1.27	-1	2	1	3	Cu$TRM	c	-1	-1	0		
3	PLUSpin	56.157	25.695	1.167	-1	2	1	3	Cu$TRM	c	-1	-1	0		
4	U10001	4.652	25.043	3.83	3.73	2	-1	-1	Comp_diel_loc$TRM	r	-1	-1	0.5		
5	U20001	20.519	12.435	2.624	3.442	2	-1	-1	Comp_diel_loc$TRM	r	-1	-1	0.5		
6	TC_U2	21.75	14.271	0.274	0.412	2	1	1	Cu$TRM	r	-1	-1	0		
7	TC_U1	6.381	26.827	0.412	0.48	2	1	1	Cu$TRM	r	-1	-1	0		
8	TC_Minus	8.525	32.378	0.755	0.572	2	1	1	Cu$TRM	r	-1	-1	0		
9	TC_Plus	53.654	25.729	0.206	0.343	2	1	1	Cu$TRM	r	-1	-1	0		
10	U3	40.617	12.762	3.156	3.156	2	0	0	Cu$TRM	r	-1	-1	0.5		

2.6 Initial and ambient conditions

- Free standing PCB without enclosure (cf. Comments)
- Free convection at 20 degC ambient temperature
- Additional air flow is neglected
- Initial temperature 20 degC

Top face Ambient temperature degC: 20 Heat exchange W/m2K: 11 Bottom face Ambient temperature degC: 20 Heat exchange W/m2K: 11	

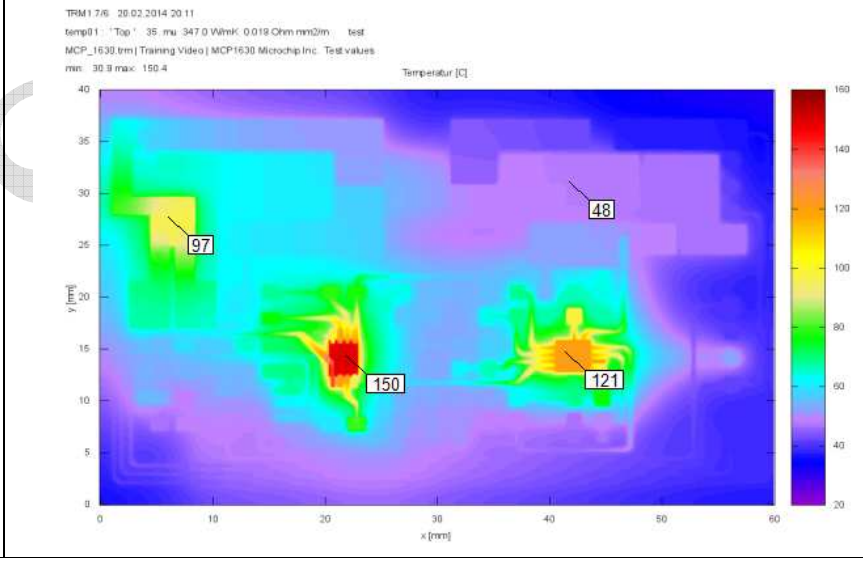
3 Results

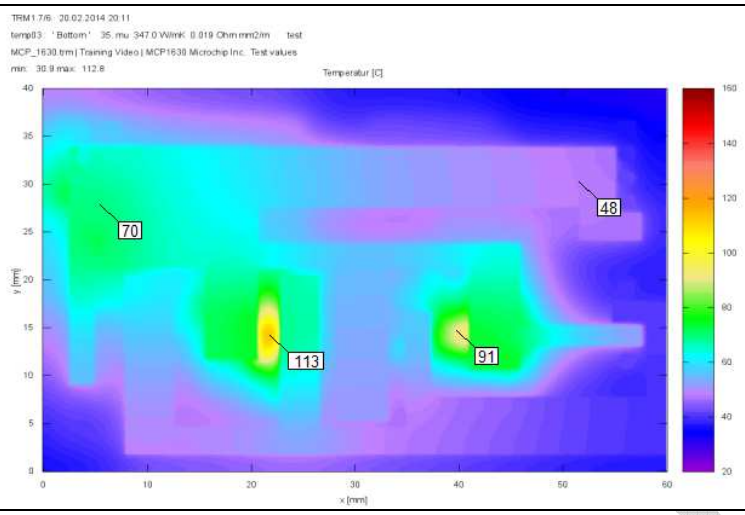
No transient analysis has been requested. The results given below are steady-state values.

3.1 Initial model „TestBoard_1“

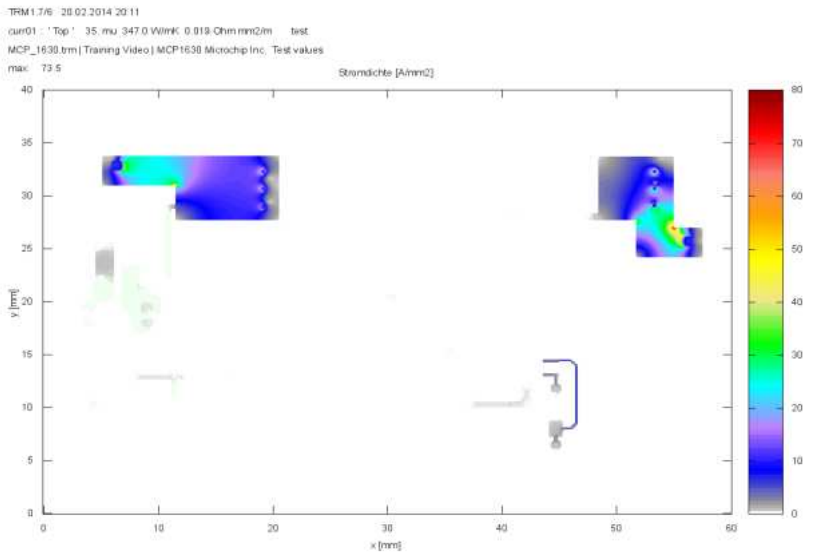
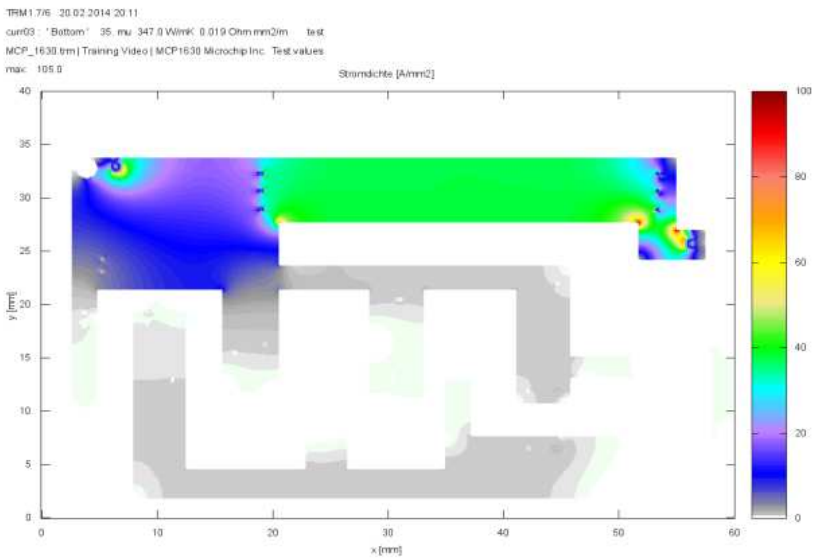
3.1.1 Temperature

- U1: 97 degC
- U2: 150 degC
- U3. 121 degC

Level		
01		Temperature (degC) Top layer

03		Temperature (degC) Bottom layer

3.1.2 Current density

01		Current density (A/mm²) Top layer
03		Current density (A/mm²) Bottom layer

… + more results if available. A complete picture gallery in a zip will be attached. Also a textual report summary will be sent.

3.2 Result Scenario 2

… …

…

4 Remarks

Components have an internal thermal architecture. This has to be checked carefully.

- If the component is designed to expel heat from the top face, then cooling and heat spreading in the board are of little influence
- Caution: if the component is designed to expel heat to the board, the fan cooler concept and the complete device design should be reinvestigated.
- …

The component temperatures bear some uncertainties.

- if air flow around board is better than free convection, the temperature will drop
- internal heat flow partitioning (top vs. Board direction) is not known.

Thin GND layers may not reduce heat removal (or increase temperature).

- Heating by electric current in traces would be affected by final layer thickness.
- Prepreg thickness is subject to manufacturing variations.
- …

Date: ….

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